REMARKS

Applicant has carefully reviewed and considered the Office Action mailed on October 24, 2002, and the references cited therewith.

Claims 1, 10, 15 and 17 are amended; as a result, claims 1-21 are now pending in this application.

Claim 1 has been amended to correct a grammatical mistake. In particular, "to" has been deleted from claim 1.

Claims 10 and 15 are amended to clarify the claims. The amendments are not intended to limit the score of equivalents to which any claim element may be entitled. In particular, "being set" is replaced by "to indicate" in claims 10 and 15.

Claim 17 has been amended to correct a grammatical mistake. A "," has been added after "buffer."

Rejections Under 35 U.S.C.§103

Claims 1-2, 4-5, and 7-8 were rejected under 35 U.S.C.§103(a) as being unpatentable over Gilbert et al. (U.S. Patent No. 6,041,376; hereinafter referred to as Gilbert) in view of Arimilli et al. (U.S. Patent No. 6,138,218; hereinafter referred to as Arimilli).

The Examiner has the burden under 35 U.S.C. § 103 to establish a *prima facie* case of obviousness. *In re Fine*, 837 F.2d 1071, 1074, 5 USPQ2d 1596, 1598 (Fed. Cir. 1988). To do that the Examiner must show that some objective teaching in the prior art or some knowledge generally available to one of ordinary skill in the art would lead an individual to combine the relevant teaching of the references. *Id.*

The *Fine* court stated that:

> Obviousness is tested by "what the combined teaching of the references would have suggested to those of ordinary skill in the art." *In re Keller*, 642 F.2d 413, 425, 208 USPQ 871, 878 (CCPA 1981)). But it "cannot be established by combining the teachings of the prior art to produce the claimed invention, absent some teaching or suggestion supporting the combination." *ACS Hosp. Sys.*, 732 F.2d at 1577, 221 USPQ at 933. And "teachings of references can be combined *only* if there is some suggestion or incentive to do so." *Id.* (emphasis in original).

The M.P.E.P. adopts this line of reasoning, stating that

> In order for the Examiner to establish a *prima facie* case of obviousness, three base criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure. *M.P.E.P.* § 2142 (citing *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed.Cir. 1991)).

In reference to independent claim 1, the Office Action asserts that Gilbert shows "setting a status flag to indicate that a bus transaction attempting to modify the shared resource is pending," (The Office Action refers to Figure 8C; column 9, lines 63-65; and column 11, lines 9-20.) At the same time though, the Office Action admits that Gilbert does not teach a status flag as a bit. Applicant respectfully submits that the cited combination does not teach or suggest every element of amended independent claim 1 for the reasons that follow.

First, claim 1 recites, "setting a status bit to indicate that a bus transaction attempting to modify the shared resource is pending." In contrast, the cited passage from Gilbert at column 9 lines 63-65 teaches a "hold flag." According to Gilbert, when the hold flag is set, "the snoopy cache protocol engine prevents other nodes or processors on the same node from accessing the data line." Therefore Gilbert's hold flag is for preventing nodes or processors from accessing a data line, but not for indicating that a bus transaction attempting to modify a shared resource is pending, as set forth in claim 1 for the reasons that follow.

Second, the Office Action further asserts that Gilbert teaches "retrying each subsequent nonmodifying bus transaction for the shared resource until the status flag is cleared." (The Office Action refers to Figure 8C; column 11, lines 9-20; and column 9, lines 14-18.) Claim 1 recites "retrying each subsequent nonmodifying bus transaction for the shared resource until the status bit is cleared." The cited passage from Gilbert at column 11, lines 9-20 teaches setting a hold-for-forward-progress field, which enables a

snoopy cache protocol engine to prevent other nodes from accessing certain data. The hold-for-forward-progress field can be used to cause nodes to retry data requests. However, this passage does not teach retrying each subsequent nonmodifying bus transaction until the status bit is cleared, as recited in claim 1.

The passage from Gilbert at column 9, lines 14-18 teaches processors "controlling" a data line by preventing other processors from reading or writing the data line. Gilbert goes on to say, "Allowing a single processor to control a data line insures multiple processors cannot write to the same data line simultaneously." Gilbert at column 9, lines 19-21. As such, this passage does not teach retrying each subsequent nonmodifying bus transaction until the status bit is cleared, as recited in claim 1.

Third, as indicated above, the Office Action admits that Gilbert does not teach "the status flag as a bit and preventing live-lock," but looks to Arimilli to teach these details. However, the only way the Office Action can teach or suggest all the elements of claim 1 is for Arimilly to teach what Gilbert is lacking. The Office Action does not cite any passage from Aramilli that teaches a status bit, and applicant knows of no such passage. Therefore, Applicant respectfully submits that the cited combination does not teach or suggest all the elements of independent claim 1 and requests that this rejection be withdrawn.

Claims 2, 4, and 5 depend, directly on claim 1 and are patentable over Gilbert and Arimilly for the reasons asserted above, plus the elements in the claims. If an independent claim is nonobvious under 35 U.S.C. § 103, then any claim depending therefrom is nonobvious. MPEP § 2143.03. Therefore, Applicant respectfully requests that this rejection be withdrawn.

In reference to independent claim 7, the Office Action asserts that Gilbert teaches the limitations of independent claim 7, except for using a status flag as a bit. Gilbert does not teach using a status bit, as set forth in independent claim 7. In particular, Gilbert does not teach "granting the cache line for the reissued first bus transaction if the status bit is set for the cache line," as set forth in independent claim 7. In rejecting independent claim 7, the Office Action relies on passages from Gilbert similar to those it cited in its rejection

of claim 1. As discussed above, the cited passages teach a hold flag and preventing processors from accessing a data line. However, these passages do not teach using a status bit, as claimed in independent claim 7 (see discussion of claim 1 above for more detail).

Claims 8 depends, directly on claim 7 and is patentable over Gilbert and Arimilly for the reasons argued above, plus the elements in the claims. If an independent claim is nonobvious under 35 U.S.C. § 103, then any claim depending therefrom is nonobvious. MPEP § 2143.03. Therefore, Applicant respectfully requests that this rejection be withdrawn.

Claims 3, 6, and 9 were rejected under 35 U.S.C.§103(a) as being unpatentable over Gilbert et al. (U.S. Patent No. 6,041,376) in view of Arimilli et al. (U.S. Patent No. 6,138,218), as applied to claims 1 and 7 above, and further in view of Donley et al. (U.S. Patent No. 5,761,446; hereinafter referred to as Donley).

Claims 3, 6, and 9 depend form one of independent claims 1 or 7. For the cited combination of Gilbert, Armilli, and Donley to teach or suggest all the limitations of these dependent claims, Donley must teach what Gilbert and Armilli are lacking. The Office Action looks to Donley for teaching generating random and pseudo-random numbers. However, the Office Action does not point to a passage in Donley that teaches a status bit as claimed in dependent claims 3, 6, and 9, and Applicant knows of no such passage. Therefore, Applicant respectfully submits that the cited combination does not teach every element of these rejected dependent claims and requests this rejection to be withdrawn.

Claims 10-21 were rejected under 35 U.S.C.§103(a) as being unpatentable over Vogt et al. (U.S. Patent No. 5,897,656; hereinafter referred to as Vogt) in view of Gilbert et al. (U.S. Patent No. 6,041,376).

In reference to amended independent claims 10 and 15, the Office Action admits that Vogt does not specifically show a status indicator that is set when a first one of the processors initiates a bus transaction attempting to modify the shared resource. The Office Action asserts that Gilbert teaches what Vogt is lacking. Amended independent claims 10 and 15 recite "a status indicator associated with each one of the plurality of

buffers, the status indicator to indicate when a first one of the processors initiates a bus transaction attempting to modify the shared resource and the bus transaction is retried." However Gilbert does not teach this limitation of claims 10 and 15. As discussed above, Gilbert teaches a hold flag and preventing processors from accessing a data line. As such, the combination of Gilbert in view of Vogt does not teach or suggest all the limitations of amended independent claims 10 and 15. Therefore, Applicant respectfully requests that this rejection be withdrawn and submits that amended independent claims 10 and 15 are in condition for allowance.

In reference to independent claim 17, the Office Action admits that Vogt does not specifically show the status indicators indicating that one of the bus transactions attempting to modify one of the cache lines is retried. The Office Action asserts that Gilbert teaches what Vogt is lacking. Independent claim 17 recites "a plurality of status indicators to indicate that one of the bus transactions attempting to modify one of the cache lines is retried, at least one of the status indicators associated with each one of the buffers." However Gilbert does not teach this limitation of claim 17. As discussed above, Gilbert teaches a hold flag and preventing processors from accessing a data line. As such, the combination of Gilbert in view of Vogt does not teach or suggest all the limitations of amended independent claim 17. Therefore, Applicant respectfully requests that this rejection be withdrawn and submits that independent claim 17 is in condition for allowance.

Claims 11-14, 16, and 18-21 depend, directly or indirectly, on claims 10, 15, and 17, respectively, and are patentable over Vogt and Gilbert for the reasons asserted above, plus the elements in the claims. If an independent claim is nonobvious under 35 U.S.C. § 103, then any claim depending therefrom is nonobvious. MPEP § 2143.03. Therefore, Applicant respectfully requests that this rejection be withdrawn.

Conclusion

Applicant respectfully submits that the claims are in condition for allowance and notification to that effect is earnestly requested. The Examiner is invited to telephone Applicant's attorney (612) 349-9592 to facilitate prosecution of this application.

If necessary, please charge any additional fees or credit overpayment to Deposit Account No. 19-0743.

Respectfully submitted,

BRIAN R. BENNETT ET AL.

By their Representatives,
SCHWEGMAN, LUNDBERG, WOESSNER
& KLUTH, P.A.
P.O. Box 2938
Minneapolis, MN 55402
(612) 349-9592

Date April 24, 2003 By Ann M. McCrackin
Ann M. McCrackin
Reg. No. 42,858

CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail, in an envelope addressed to: Commissioner of Patents, Washington, D.C. 20231, on this 24th day of April 2003.

Name ANN MCCRACKIN Signature Ann M. McCrackin